IN THE CLAIMS:

Please amend Claims 32 and 47 and add new Claims 50 and 51 as follows.

Claims 1-31. (Cancelled).

32. (Currently Amended) An image display apparatus comprising:

a plurality of display devices wired in a matrix through a plurality of scanning signal wirings and a plurality of modulated signal wirings; and

a driving circuit configured to apply a modulated signal having a modulated pulsewidth to each of said plurality of modulated signal wirings,

wherein said driving circuit has a plurality of transistors connected in parallel to one of the plurality of modulated signal wirings, wherein the plurality of transistors include a first transistor and a second transistor, and a duration of a time period in which the first transistor is in an on state and a duration of a time period in which the second transistor is in an on state are different from each other.

Claims 33 and 34. (Cancelled).

35. (Previously Presented) The apparatus according to claim 32, wherein at least one of the plurality of transistors is connected to a predetermined potential.

Claims 36-38. (Cancelled).

39. (Previously Presented) The apparatus according to claim 32, further comprising a circuit for determining the operation states of the plurality of transistors.

40. (Previously Presented) The apparatus according to claim 32, wherein said driving circuit comprises a rise circuit for raising the signal level of the modulated signal and a fall circuit for causing the signal level of the modulated signal to fall.

41. (Previously Presented) The apparatus according to claim 32, wherein each said display device comprises an electron-emitting device.

Claims 42-46. (Cancelled).

47. (Currently Amended) An image display apparatus, comprising:

a plurality of display devices wired in a matrix through a plurality of scanning signal wirings and a plurality of modulated signal wirings; and

a driving circuit configured to apply a pulse signal as a modulated signal having a modulated pulsewidth to each of the plurality of modulated signal wirings,

wherein at least one pulse signal has a first portion at the leading edge of the pulse signal and a second portion at the trailing edge of the pulse signal, wherein

in the first portion, a signal level of the pulse rises up to a first predetermined level which is lower than a maximum level of the pulse signal and is maintained at the first predetermined level during a first predetermined time period, and wherein

in the second portion, a signal level of the pulse falls down to a second predetermined level which is lower than the maximum level of the pulse signal and is maintained at the second predetermined level during a second predetermined time period.

Claims 48 and 49. (Cancelled).

50. (New) An apparatus according to claim 32, wherein the time period in which the first transistor is in the on state partially overlaps the time period in which the second transistor is the on state.

51. (New) An apparatus according to claim 47, wherein the first predetermined level is equal to the second predetermined level.